1. (previously amended) A system for inductance testing a plurality of planar magnetic circuits, comprising:

a substrate;

a plurality of cores spaced and electrically isolated from one another and mounted on said substrate, wherein each one of said plurality of cores registers with a corresponding one of said plurality of planar magnetic circuits;

a carriage moveable on one or more axes with respect to said plurality of planar magnetic circuits;

a pair of leads, wherein said leads are mounted to said carriage;

a controller, which coordinates the actions of said carriage and said leads so as to implement testing;

wherein said controller selects one of said plurality of planar magnetic circuits and contacts said pair of leads with said selected planar magnetic circuit and delivers an electrical current through said selected planar magnetic circuit while the corresponding registered core enhances inductance in said selected planar magnetic circuit;

wherein, after said selected planar magnetic circuit is tested, said controller positions the leads so that another planar magnetic circuit may be tested; and

an inductance measuring tool.

2. (original) A system according to claim 1, further comprising a plurality of beds in said substrate for registering said plurality of planar magnetic circuits with said plurality of cores.

3-8. (canceled)

9. (currently amended) A method for inductance testing a board having a planar magnetic circuit and a pair of contacts, comprising the steps of:

providing a substrate having an electrically isolated core and bed;

loading said board on said bed to register said planar magnetic circuit with said core;

providing a pair of leads and a plate;

contacting said pair of leads with said pair of contacts and said plate with said core using a controller;

delivering an electrical current through said planar magnetic circuit while said plate and said core enhance inductance in said planar magnetic circuit;

measuring inductance in said planar magnetic circuit; and

determining whether said inductance is in a predetermined range, and

marking said board if said inductance is not in said predetermined range.

10. (canceled)

11. (original) A method according to claim 9, further comprising:

analyzing said board to identify a defect if said inductance is not in said predetermined range; and improving a design of said board to overcome said defect.

12-19. (canceled)

20. (currently amended) A method according to claim ~~10~~ 9 wherein said marking step is accomplished by drilling said board to prevent use of said board and to provide a visible indicator of the non-functional condition of the board.